Compact Headphone Amplifiers

Headphone Amplifier Designed for 0.93V Low Voltage Operation

BU7150NUV

No.11102EDT01

●Description

BU7150NUV is Audio Amplifier designed for Single-cell battery operated audio products (VDD = 0.93 ~ 3.5V, at Ta=0~85°C). BU7150NUV can be selected in single-ended mode for stereo headphone and BTL mode for mono speaker operations. For BU7150NUV at VDD = 1.5V, THD+N = 1%, the output power is 14mW at RL = 16Ω in single-ended mode and the output power is 85mW at RL = 8Ω in BTL mode.

●Features

1) Wide battery operation Voltage (0.93V~3.5V, Ta=0~85°C) (1.03V~3.5V, Ta= -40~85°C)
2) BU7150NUV can be selected in single-ended mode for stereo headphone and BTL mode for mono speaker operation
3) Unity-gain stability
4) Click and pop-noise reduction circuit built-in
5) Shutdown mode(Low power mode)
6) High speed turn-on mute mode
7) Thermal shutdown protection circuit
8) Power-on reset circuit not sensed during start-up slew rate of supply voltage
9) Small package (VSON010V3030)

●Applications

Noise-canceling headphone, IC recorder, Mobile phone, PDA, Electronic toys etc..

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply Voltage	VDD	4.5	V
Input Voltage	VIN	VSS-0.3~VDD+0.3	V
Input Current	IIN	-10~10	mA
Power Dissipation	PD	560 *	mW
Storage Temperature Range	TSTG	-55~+150	°C

*For operating over 25°C, de-rate the value at 5.6mW/°C.
This value is for IC mounted on 74.2 mm x 74.2mm x 1.6mm glass-epoxy PCB of single-layer.

●Operating conditions

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Operation Temperature Range	TOPR	-40	-	85	°C
Supply Voltage (Note 1,2)	VDD	0.93	-	3.5	V

Note 1: If the supply voltage is 0.93V, BU7150NUV does not operate at less than 0°C.
If the supply voltage is more than 1.03V, BU7150NUV operates until -40°C.
(But, it is not the one which guarantees the standard value for electric characteristics.)
Note 2: Ripple in power supply line should not exceed 400mV_{P-P}.(VDD=1.5 V, Ta=25°C)

●Electrical characteristics

Ta=25°C, VDD=1.5V, f=1kHz, VSS=GND unless otherwise specified.

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
No Signal Operating Current	IDD	-	1	1.4	mA	No load, No signal
Shutdown Current	ISD	-	3	9	μA	SDB Pin=VSS
Mute Current	IMUTE	-	15	-	μA	MUTEB Pin=VSS, SE
Output Offset Voltage	VOFS	-	5	50	mV	| VOUT1 – VOUT2 |, No signal
Maximum Output Power	PO	70	85	-	mW	RL=8Ω, BTL, THD+N=1%
		-	14	-	mW	RL=16Ω, SE, THD+N=1%
Total Harmonic Distortion +Noise	THD+N	-	0.2	0.5	%	20kHz LPF, RL=8Ω, BTL, PO=25mW
		-	0.1	0.5	%	20kHz LPF, RL=16Ω, SE,PO=5mW
Output Voltage Noise	VNO	-	10	-	μV_{rms}	20kHz LPF + A-weight
Crosstalk	CT	-	85	-	dB	RL=16Ω, SE, 1kHz BPF
Power Supply Rejection Ratio	PSRR	-	62	-	dB	Ripple voltage=200mV_{P-P}, RL=8Ω, BTL, C_{BYPASS}=4.7μF
		-	66	-	dB	Ripple voltage=200mV_{P-P}, RL=16Ω, SE, C_{BYPASS}=4.7μF
Input Logic High Level	VIH	0.7	-	-	V	MUTEB Pin, SDB Pin
Input Logic Low Level	VIL	-	-	0.3	V	MUTEB Pin, SDB Pin

"BTL" is BTL-mode when MODE Pin = VDD, "SE" is single-ended mode when MODE Pin = VSS.
Turn-on time in BTL mode is about 11 times faster than single-ended mode.
Also, BTL mode does not have MUTE mode. When MUTEB Pin = VSS, then it will be shutdown mode.

●Block diagram

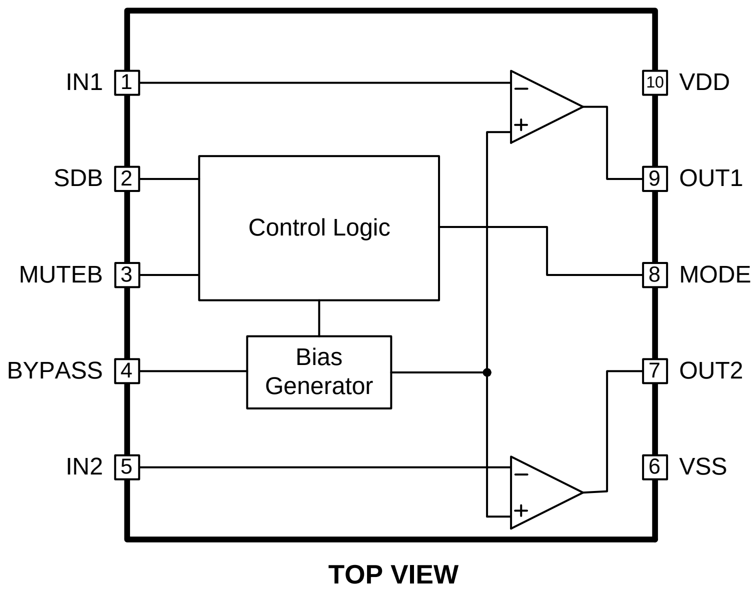


Fig. 1 Block diagram

●**Electrical characteristics waveform (Reference data)**

Ta=25°C, f=1kHz, VSS=GND unless otherwise specified. Using circuits are Fig.34 and Fig.35.
Also, RL=16Ω for single ended mode, RL=8Ω for BTL mode）

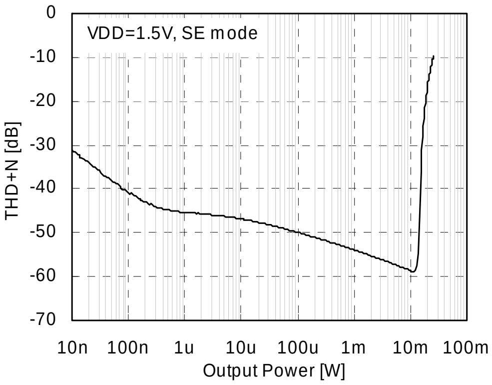


Fig. 2 THD+N vs. Output Power

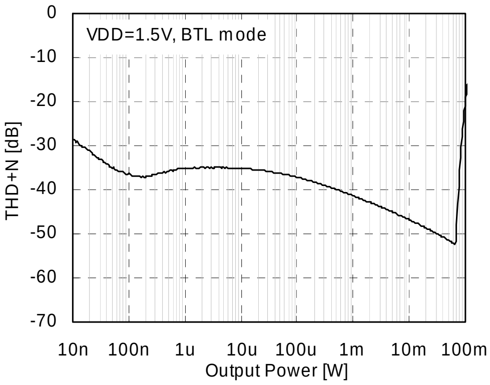


Fig. 3 THD+N vs. Output Power

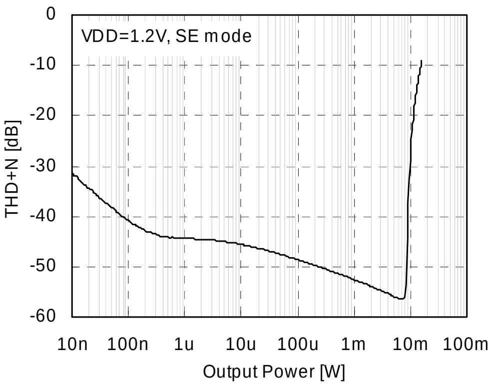


Fig. 4 THD+N vs. Output Power

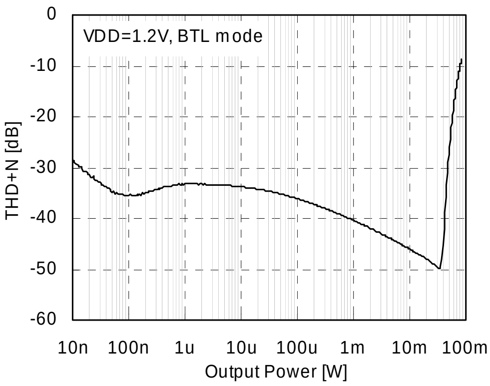


Fig. 5 THD+N vs. Output Power

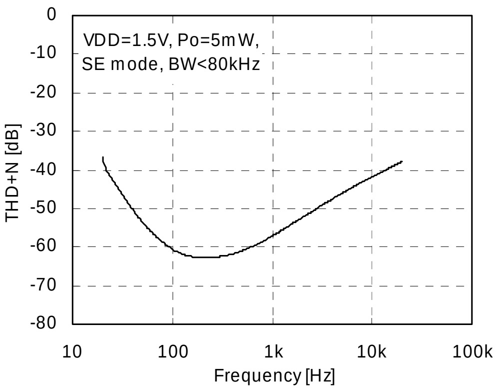


Fig. 6 THD+N vs. Frequency

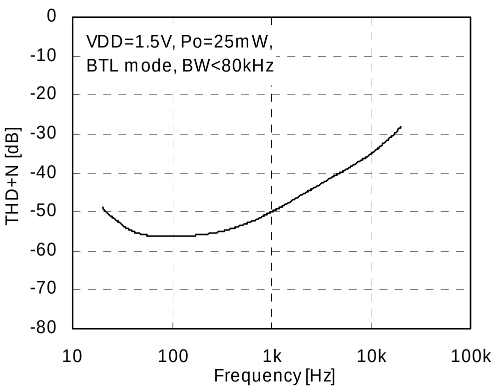


Fig. 7 THD+N vs. Frequency

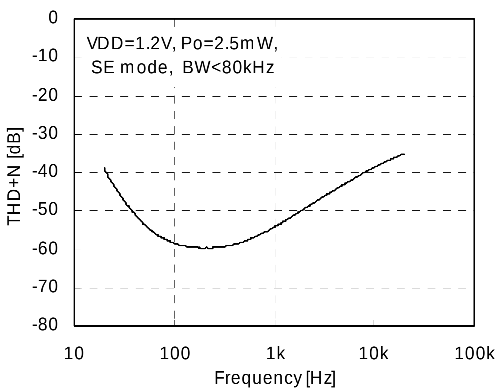


Fig. 8 THD+N vs. Frequency

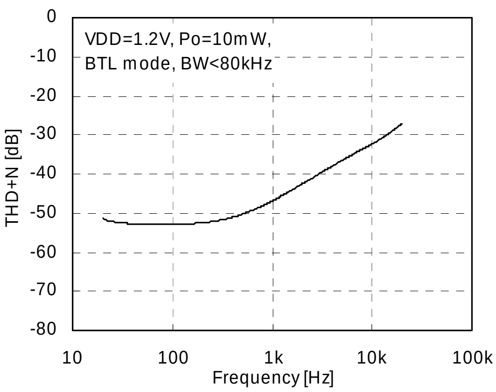


Fig. 9 THD+N vs. Frequency

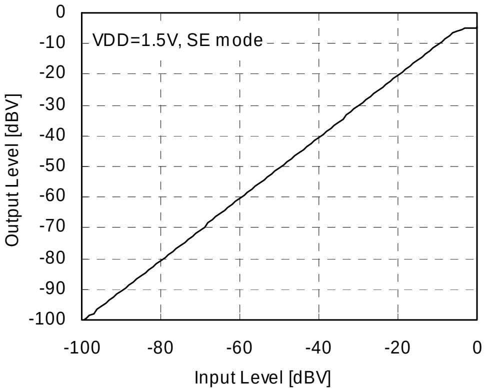


Fig. 10 Output Level vs. Input Level

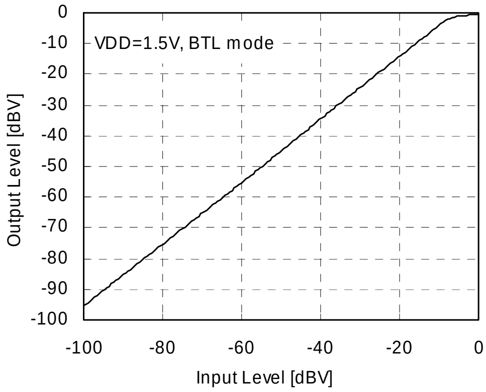


Fig. 11 Output Level vs. Input Level

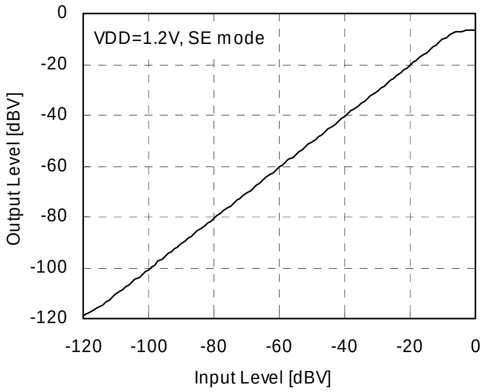


Fig. 12 Output Level vs. Input Level

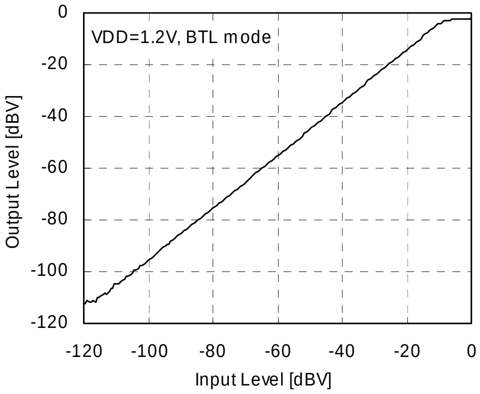


Fig. 13 Output Level vs. Input Level

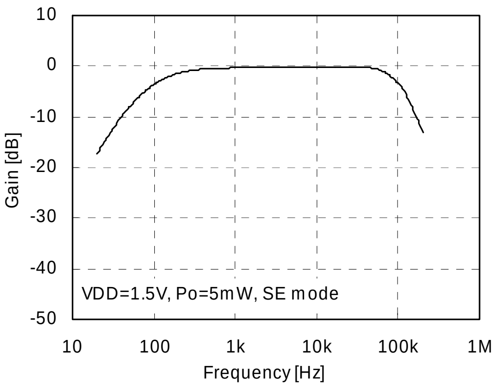


Fig. 14 Gain vs. Frequency

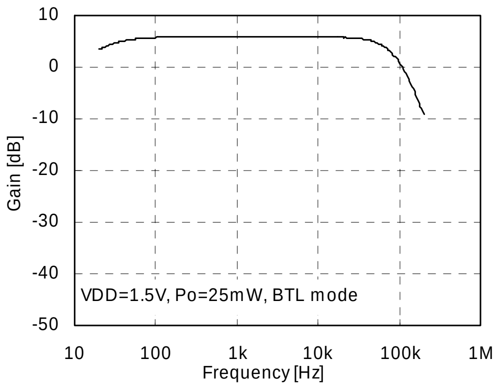


Fig. 15 Gain vs. Frequency

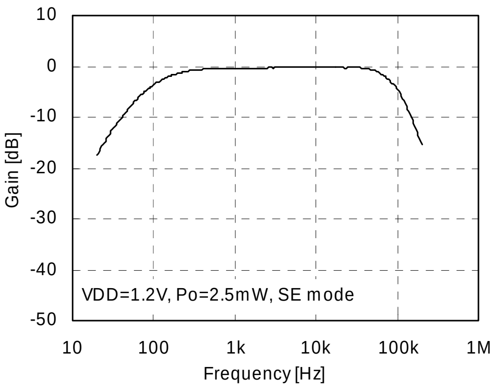


Fig. 16 Gain vs. Frequency

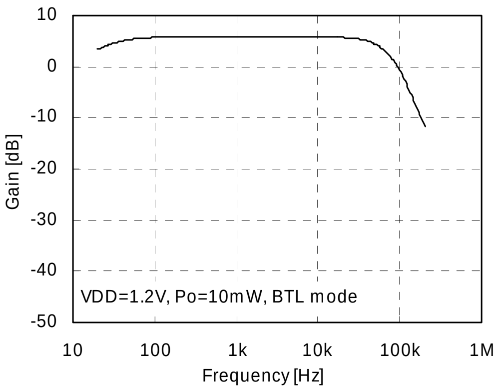


Fig. 17 Gain vs. Frequency

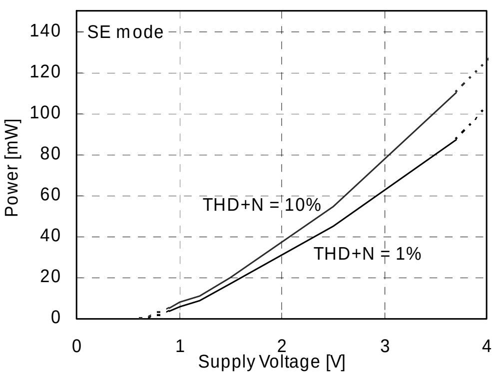


Fig. 18 Maximum output Power vs. Supply Voltage

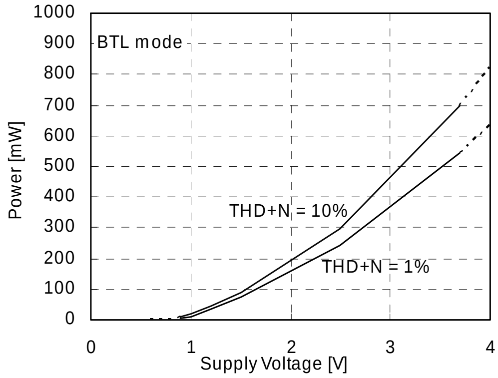


Fig. 19 Maximum output Power vs. Supply Voltage

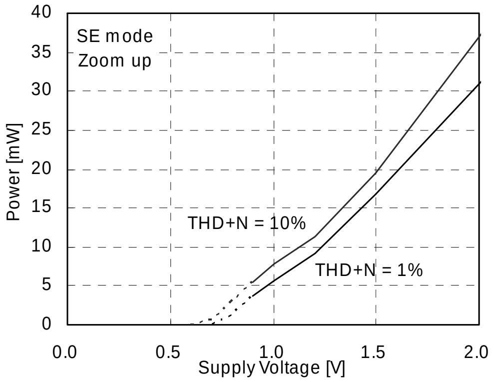


Fig. 20 Maximum output Power vs. Supply Voltage

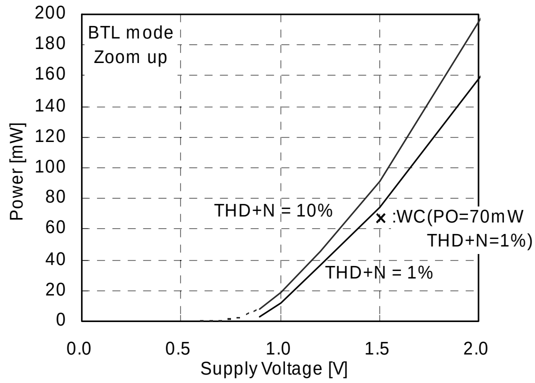


Fig. 21 Maximum output Power vs. Supply Voltage

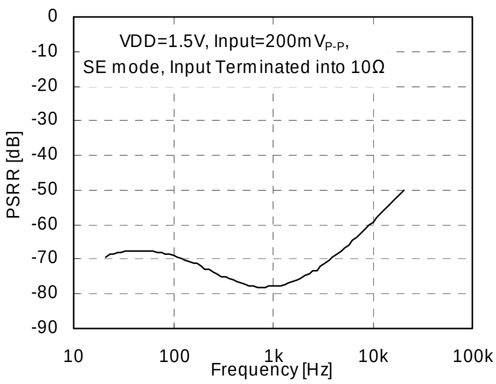


Fig. 22 PSRR vs. Frequency

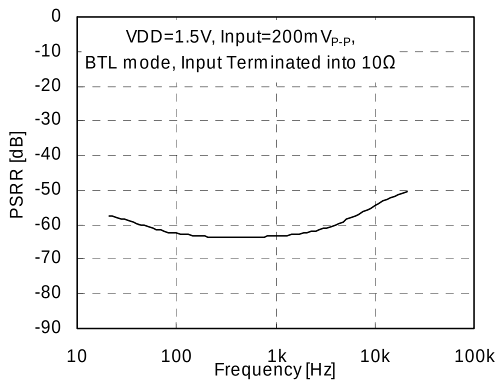


Fig. 23 PSRR vs. Frequency

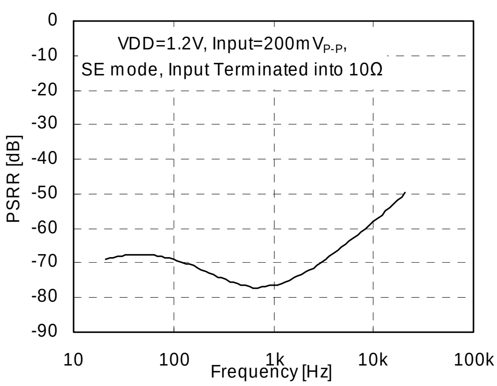


Fig. 24 PSRR vs. Frequency

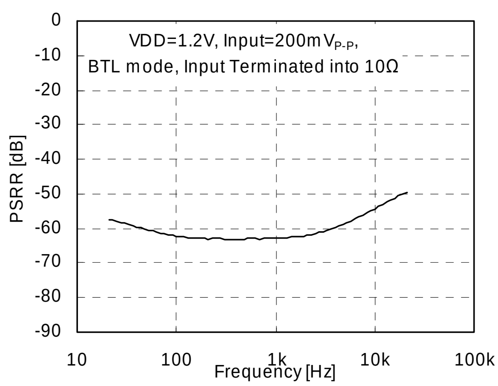


Fig. 25 PSRR vs. Frequency

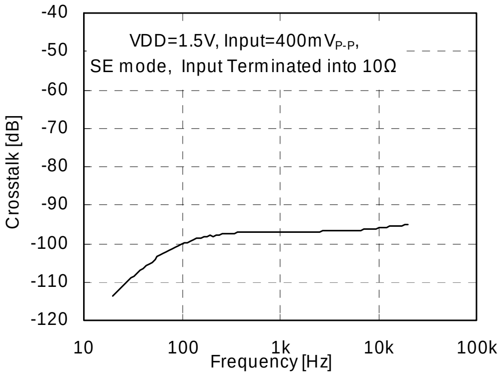


Fig. 26 Crosstalk vs. Frequency

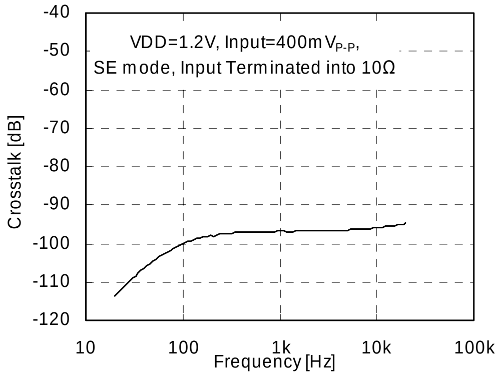


Fig. 27 Crosstalk vs. Frequency

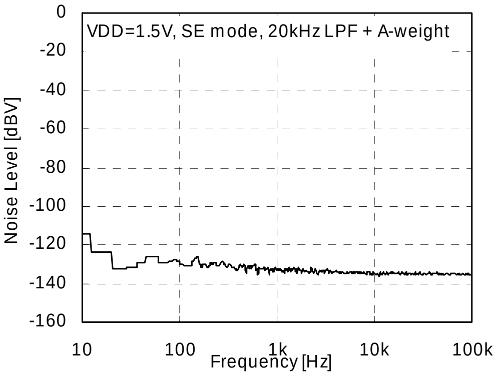


Fig. 28 Noise Level vs. Frequency

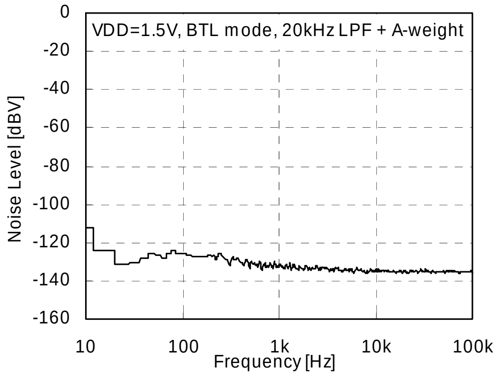


Fig. 29 Noise Level vs. Frequency

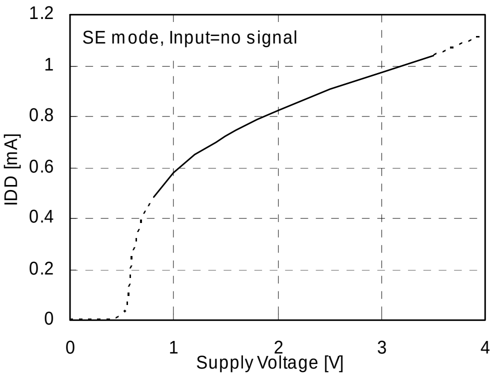


Fig. 30 IDD vs. Supply Voltage

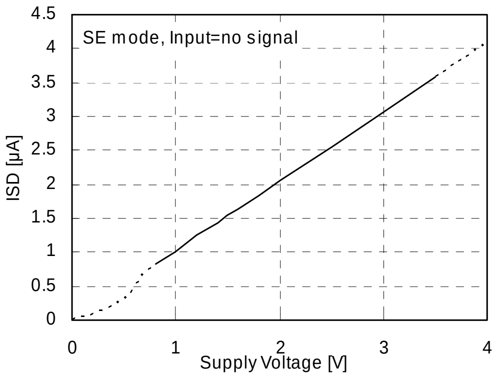


Fig. 31 ISD vs. Supply Voltage

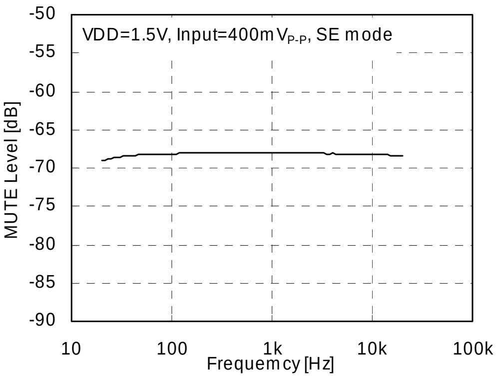
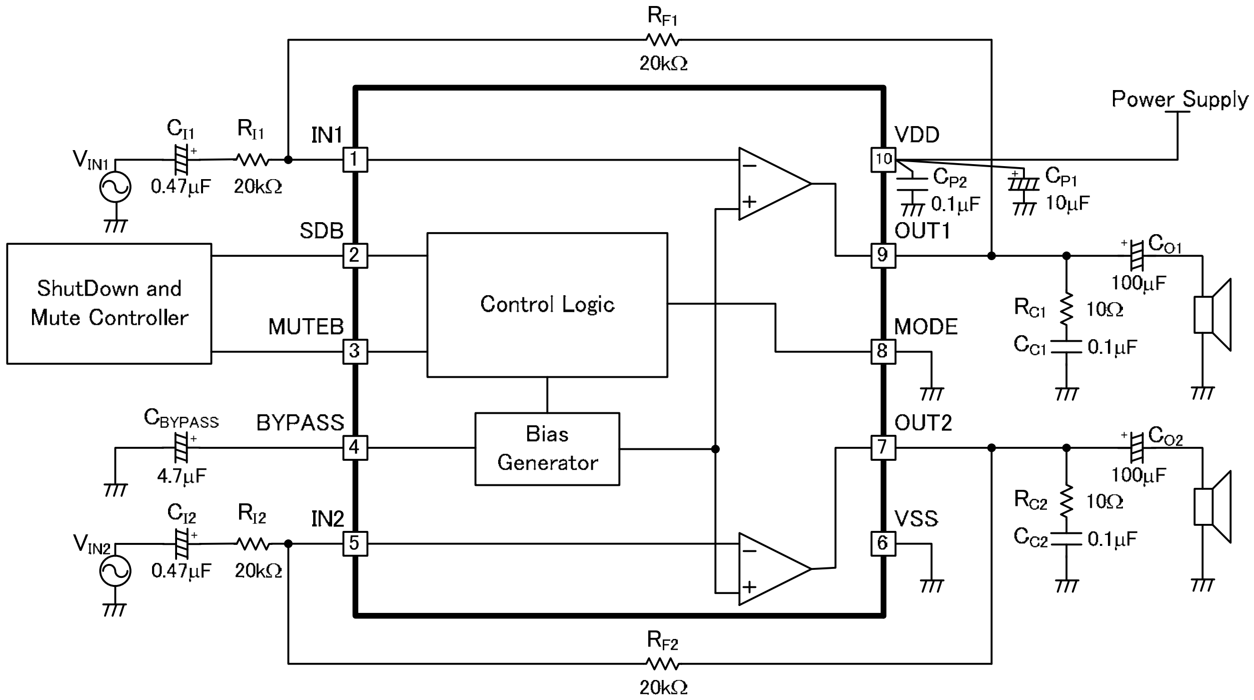


Fig. 32 MUTE Level vs. Frequency

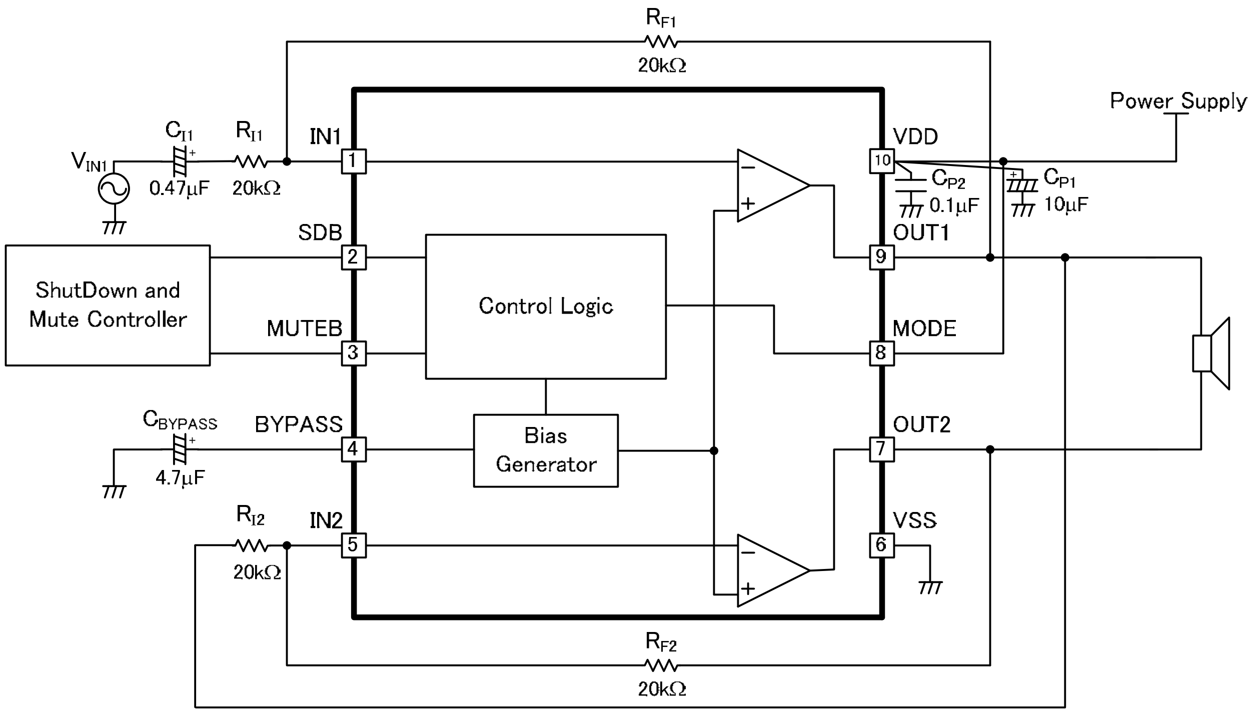
●Application Circuit



・Resistors R_{F1}, R_{F2} should be used in 20kΩ～1MΩ range.

・For gain setting greater than 4 times, then R_{C1}, R_{C2}, C_{C1}, C_{C2} can be eliminated.

Fig. 34 Single-ended mode application circuit



・Resistors R_{F1}, R_{F2} should be used in 20kΩ～1MΩ range

Fig. 35 BTL mode application circuit

●Pin Configuration

No.	Pin Name	Function	I/O equal circuit
1	IN1	Input Pin 1	A
2	SDB	Shutdown Pin (OFF at L)	C
3	MUTEB	Mute Pin (Mute at L)	C
4	BYPASS	Bypass Pin	D
5	IN2	Input Pin 2	A
6	VSS	GND Pin	-
7	OUT2	Output Pin 2	B
8	MODE	Mode Select Pin (SE at VSS, BTL at VDD)	A
9	OUT1	Output Pin 1	B
10	VDD	Power Supply Pin	-

●I/O equal circuit (Fig. 36)

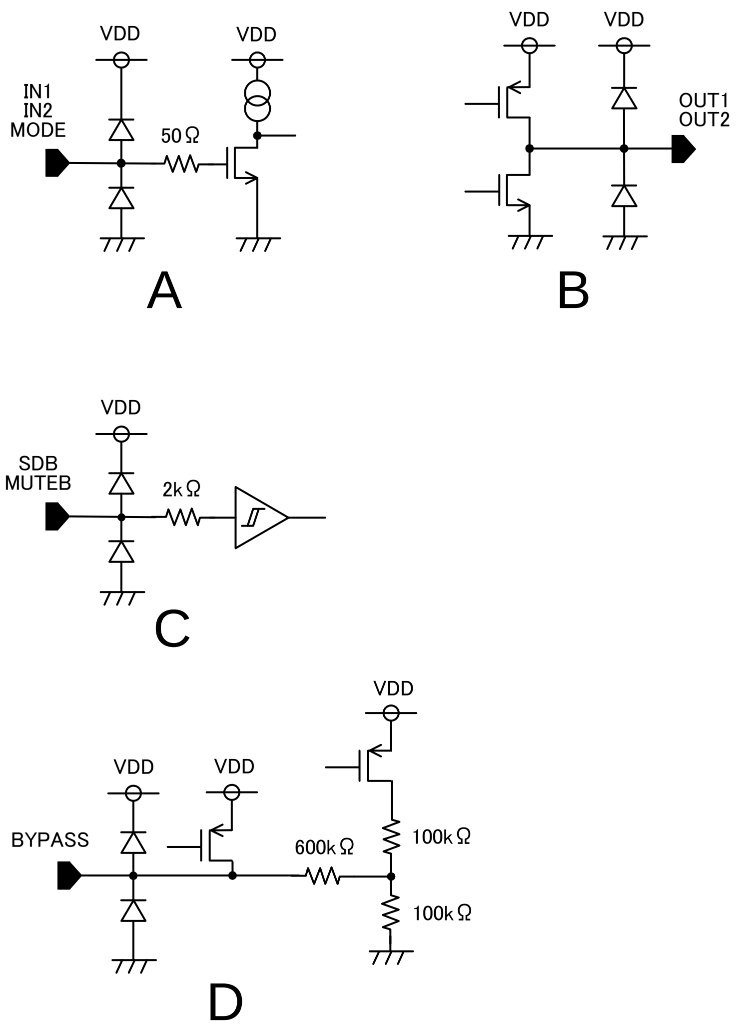


Fig.36 I/O equal circuit

●Functional descriptions

[Timing Chart]

BU7150NUV can control many mode states. “Active” is normal operation state for output signal. “Shutdown” is IC power down state for low power. “Mute” is Headphone amplifier power down state for low power and fast turn-on, because keeping BIAS voltage = VDD/2. “Turn on” and “Turn off” are sweep state.

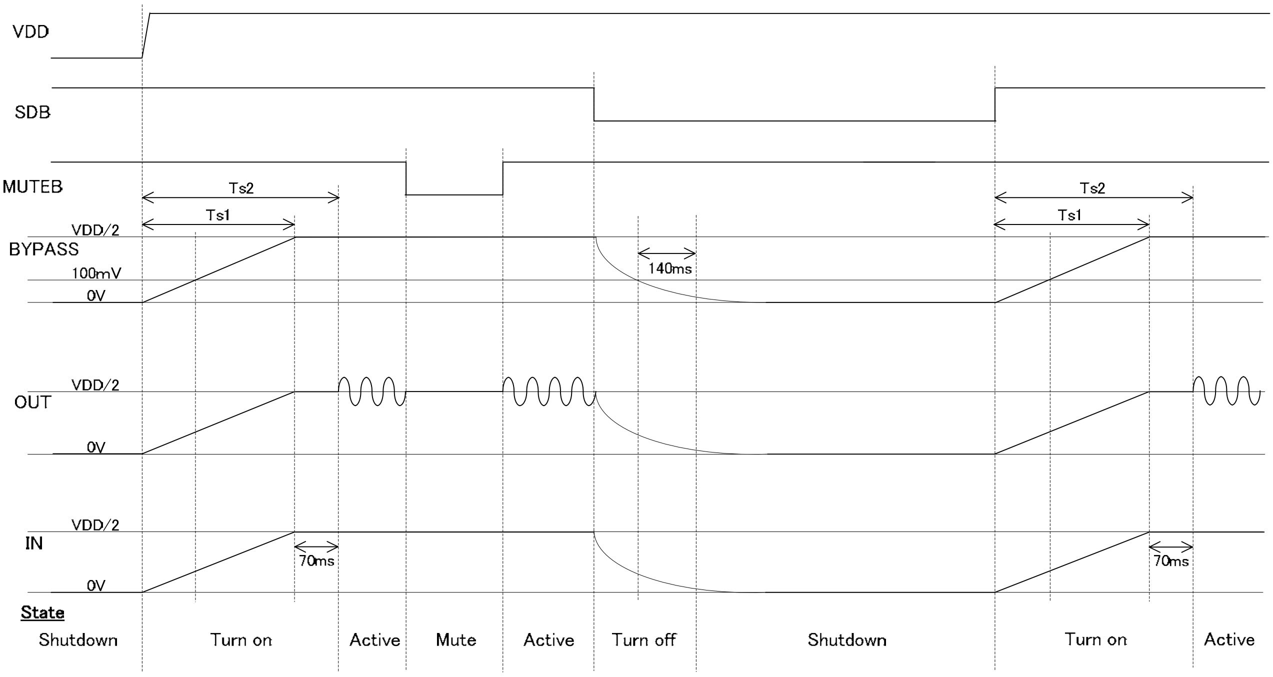


Fig. 37 Timing Chart (MODE = VSS: Single-ended mode)

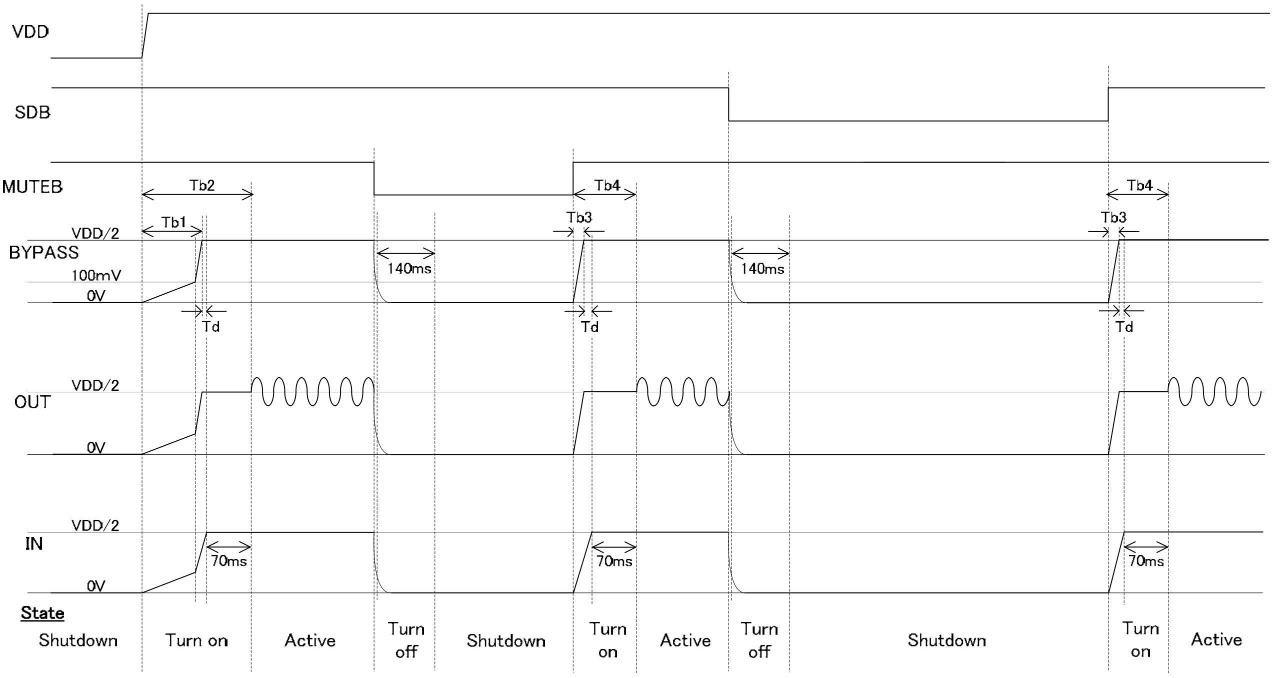


Fig. 38 Timing Chart (MODE = VDD: BTL- mode)

Also, BU7150NUV has wait time for reduction of pop-sound at turn-on and turn-off. Turn-on wait time is 70msec from IN1 voltage = VDD/2. Turn-off wait time is 140msec from BYPASS voltage = 100mV. Please don't change SDB, MUTEB condition at 70msec and 140msec wait- time.

[About Time until Signal Output]

BU7150NUV need wait-time for BIAS charge sweep time and pop-noise reduction.
In the Fig. 37, Ts1 is BIAS charge sweep time from power on or SDB=H. Ts2 is time until signal output from power on or SDB=H. Also, in the Fig. 38, Tb1 is BIAS charge sweep time from power on. Tb2 is time until signal output from power on. Tb3 is BIAS charge sweep time from SDB=H. Tb4 is time until signal output from SDB=H.
These values are decided equation (1) ~ (6). However, BIAS charge sweep time (Ts1, Tb1, Tb3) have uneven ±50%, and wait-time (70msec) is 40msec ~ 126msec for process parameter distribution. (Ta=25°C)

$$Ts1 = \frac{VDD \times C_{BYPASS}}{2.5 \times 10^{-6}} [sec] \quad \cdots \quad (1)$$

$$Ts2 = Ts1 + 0.07[sec] \quad \cdots (2)$$

$$Tb1 = \frac{(VDD + 2) \times C_{BYPASS}}{27.5 \times 10^{-6}} [sec] \quad \cdots \quad (3)$$

$$Tb2 = Tb1 + 0.07[sec] \quad \cdots (4)$$

$$Tb3 = \frac{VDD \times C_{BYPASS}}{27.5 \times 10^{-6}} [sec] \quad \cdots \quad (5)$$

$$Tb4 = Tb3 + 0.07[sec] \quad \cdots (6)$$

In the Fig. 38, Tb1 and Tb3 is differ value, because BU7150NUV's default is single-ended mode. BU7150NUV need BYPASS>100mV to recognize for BTL mode.
Also, Td is delay time to C_{I1}=VDD/2 from BYPASS=VDD/2. Td is decided by C_{I1}, R_{I1}, and R_{F1}.

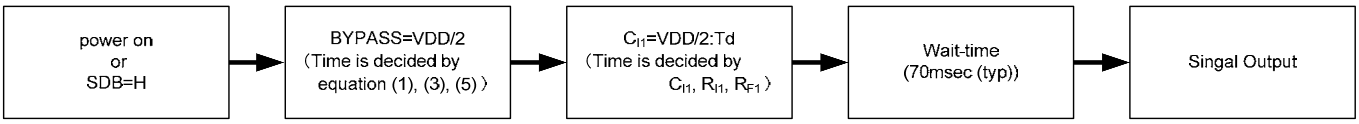


Fig. 39 Flow of Time until Signal Output

[Operation mode]

・Selecting operation mode

BU7150NUV has two OPAMP in the IC (Fig. 1). BU7150NUV is selected for BTL-mode for mono speaker and single-ended mode for stereo headphone operation. Mode is composed of external parts and internal control (Fig. 34, 35) BU7150NUV operates at single-ended mode when MODE pin (pin8) = 0V turn on. BTL mode is operated when MODE pin (pin8) = VDD turn on. BYPASS voltage = 100mV then operation mode is decided by internal comparator by detecting MODE voltage.

The difference between Single-ended mode and BTL-mode is mentioned in the following table.

Parameter	Single ended mode MODE='VSS'	BTL mode MODE='VDD'
Mute function	enable	disenable
Bypass voltage turn on time [Ts1, Tb1, Tb3] (C_{BYPASS}=4.7μF)	Ts1=2.82sec	Tb1=598msec Tb3=256msec
Time until Signal Output [Ts2, Tb2, Tb4](C_{BYPASS}=4.7μF)	Ts2=2.89sec	Tb1=668msec Tb3=326msec
Maximum Output Power (THD=1%)	14mW	85mW
Total Harmonic Distortion + Noise	0.10%	0.20%
Power Supply Rejection Ratio	66dB	62dB

(Ta=25℃, VDD=1.5V, f=1kHz)

・Single-Ended mode

Single-ended mode can be use for stereo headphone amplifier using two internal amplifiers. BU7150NUV can select amplifier gain A_v using external parts. (Fig. 34) Two amplifiers gain A_v is decided by input resistance R_{I1}, R_{I2} and feedback resistance R_{F1}, R_{F2} aspect. Also, Please, use R_{F1}, R_{F2} value in the range 20kΩ~1MΩ.

$$A_V = -\frac{R_F}{R_I}$$

Amplifier outputs (OUT1, OUT2) need coupling capacitors in single-ended mode operation. Coupling capacitors reduce DC-voltage at the output and to pass the audio signal.
Single-ended mode has mute mode. Mute mode reduces pop noise and low power (typ. 15µA) when MUTEB pin = Low. Rise time is high-speed though current consumption increases more than the state of the shutdown so that the state of the mute may keep the output level at the bias level. Mute level is decided by input resistance R_{I1}, R_{I2} and feedback resistance R_{F1}, R_{F2} and R_L

$$\text{Mute level [dB]} \quad = 20\mathrm{Log}\frac{R_L}{R_I + R_F}$$

BU7150NUV needs phase-compensation circuit using external parts. (Fig. 34) But, for amplifier gain Av > 4 then phase compensation circuit may be eliminated.

・BTL mode

BTL mode can be used for mono speaker amplifier using two internal amplifiers. BU7150NUV can select amplifier gain A_v using external parts. (Fig. 35) 1st stage gain is decided by selecting external parts. But 2nd stage gain = 1. 1st stage output signal and 2nd stage output signal are of same amplitude but phase difference of 180°.
Amplifiers gain A_v is decided by input resistance R_{I1} and feedback resistance R_{F1} aspect. Also, Please, use R_{F1}, R_{F2} value in range of 20kΩ~1MΩ.

$$A_V = 2 * \frac{R_{F1}}{R_{I1}}$$

BU7150NUV has no output pop noise at BTL mode operation, because output coupling capacitor is not charged. Therefore, BTL mode is faster by 11 times compared to single-ended mode. SDB pin and MUTEB pin are same function in BTL mode operation.

[About Maximum Output Power]

Maximum output power of audio amplifier is reduced line impedance. Please, design to provide low impedance for the wiring between the power source and VDD pin of BU7150NUV. Also, please design to provide low impedance for the wiring between the GND and VSS pin of BU7150NUV.

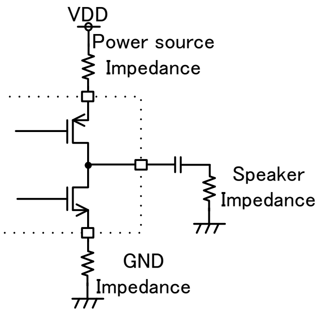


Fig. 40 Line Impedance

[How to select external parts for application]

・Power supply capacitor

Power supply capacitor is important for low noise and rejection of alternating current. Please use 10μF electrolytic or tantalum capacitor for low frequency and 0.1μF ceramic capacitor for high frequency nearer to BU7150NUV.

・BYPASS pin capacitor

BU7150NUV sweeps "Active" state after 70msec wait time after IN1 voltage = VDD/2. IN1 voltage are subordinated BYPASS voltage Ts. BYPASS voltage is subordinated BYPASS pin capacitor C_{BYPASS}. Therefore, High speed turn on time is possible if C_{BYPASS} is small value. But, pop noise may occur during turn on time. Therefore, C_{BYPASS} need to be selected best value for application.

●Notes for use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) About the rush current
For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

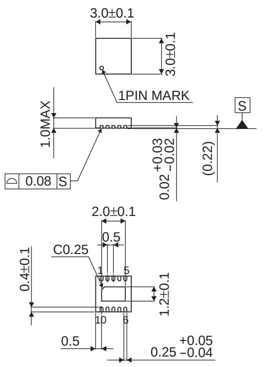
(13) Others
In case of use this LSI, please peruse some other detail documents, we called ,Technical note, Functional description, Application note.

●Ordering part number

B	D		7	1	5	0		N	U	V	-	E	2

- **B D** — Part No.
- **7 1 5 0** — Part No.
- **N U V** — Package
NUV : VSON010V3030
- **E 2** — Packaging and forming specification
E2: Embossed tape and reel

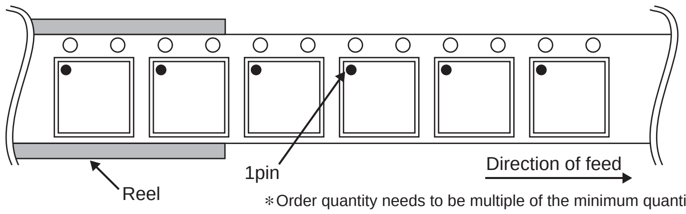
VSON010V3030



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※Order quantity needs to be multiple of the minimum quantity.

Notes

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